REMARKS

In the Office Action dated July 17, 2003, claims 1-30 were rejected under 35 U.S.C. § 103 over U.S. Patent No. 6,076,139 (Welker) in view of U.S. Patent No. 6,026,464 (Cohen). As amended, the claims are clearly allowable over the asserted combination of Welker and Cohen.

Claim 1 recites a plurality of memory controllers each to generate memory requests on a memory bus according to a predetermined priority scheme, with the predetermined priority scheme defining time slots. The memory controllers are allocated to respective time slots according to the predetermined priority scheme. Such a predetermined priority scheme is not disclosed or suggested by either Welker or Cohen. Welker does not disclose plural memory controllers on *a* memory bus--therefore, Welker would have no need for the predetermined priority scheme recited in claim 1. This is an indication that there is no motivation or suggestion to modify the teachings of Welker in the manner proposed by the Office Action. In Welker, only one memory controller (MIC 310 shown in Figure 3 of Welker) is provided on each Rambus channel. There does not exist any need in Welker for the arbitration mechanism disclosed in Cohen, because the one MIC connected to each Rambus channel as disclosed in Welker does not need to perform arbitration for the Rambus channel, since there is only one MIC connected per Rambus channel. Therefore, Applicant respectfully submits that a person of ordinary skill in the art would not have been motivated to combine the teachings of Welker and Cohen in the manner proposed by the Office Action.

Furthermore, neither Welker nor Cohen teaches or suggests the predetermined priority scheme of claim 1, where time slots are allocated to respective memory controllers. As noted above, only one MIC is connected to each Rambus channel in Welker—therefore, no predetermined priority scheme is disclosed or suggested by Welker for access by the MIC to the Rambus channel. Cohen describes a request/grant arbitration scheme, where a memory controller that needs access to a memory bus asserts a request signal, with an arbiter asserting a grant signal to enable the memory controller to access the bus. Such a request/grant arbitration scheme is different from a priority scheme defining time slots allocated to respective memory controllers.

Therefore, even if the teachings of Welker and Cohen can be combined, such combination does not teach or suggest the subject matter of claim 1.

Independent claim 23 is similarly allowable over the asserted combination of Welker and Cohen, since the asserted combination does not teach or suggest generating memory request on a memory bus according to a time slot priority scheme that defines time slots allocated to respective memory controllers.

Independent claim 10 recites a system having a plurality of memory buses and a hub connected to the plurality of memory buses. A plurality of memory controllers are connected to a first one of the memory buses, with each memory controller to monitor memory requests generated by another memory controller in performing memory-related actions. In addition, claim 10 recites that the memory controllers are able to access a second one the memory buses through the hub. The MICs 310 in the memory interface 200 (Figures 3) of Welker do not monitor memory requests generated by another memory controller in performing memory-related actions. Also, both Welker and Cohen fail to disclose or suggest a hub that is connected to a plurality of memory buses, where memory controllers are able to access a second one of the memory buses through the hub. Therefore, the asserted combination of Welker and Cohen (even if proper) does not teach or suggest the subject matter of claim 10. Furthermore, as noted above, it is improper to combine the teachings of Welker and Cohen as there is no motivation or suggestion to perform such combination.

Independent claim 15 is also allowable over the asserted combination of Welker and Cohen. Claim 15 recites a method that includes memory controllers generating requests on memory buses connected by a hub, with each memory controller monitoring memory-related actions on the memory buses by at least another memory controller. The asserted combination of Welker and Cohen does not teach or suggest such features.

In view of the foregoing, all independent clams are allowable over the cited references. Dependent claims are allowable for at least the same reasons as corresponding independent claims.

Allowance of all claims is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account No. 50-1673 (9295).

Respectfully submitted,

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Date

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